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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,489	03/04/2002	Ranjit S. Oberoi	5681-14000	5065

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EXAMINER	
LEE, HWA C	

ART UNIT	PAPER NUMBER
2672	5

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,489	OBEROI ET AL.	
	Examiner	Art Unit	
	Hwa C Lee	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 March 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims

1. Whenever appropriate, the examiner's explanations for rejecting a particular claim are attached enclosed by {}, and the citations to the prior art references used to reject the respective claim are attached enclosed by ().

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 5, 7, and 9 are rejected under 35 U.S.C. 102(a) as being anticipated by Brunner et al., U.S. Patent No. 6,369,830.

In reference to claim 1, Brunner et al. discloses the limitations of

(a) "*a system*" comprising "*an accumulation buffer*" in the following:

- For each pixel in the destination bitmap, the present invention processes the layers having a corresponding pixel...accumulating color and alpha values (col. 2, lines 34-37). {'Accumulating color and alpha values' interpreted broadly as "*an accumulation buffer*"}.
- Accumulator, in one embodiment, is a register or memory location for temporary storage of values being calculated (col. 3, lines 64-66 and Fig. 1, no. 102). {'Accumulator' is interpreted broadly as "*an accumulation buffer*"}.

(b) "*an image buffer*" in the following:

- The present invention renders two or more overlapping layers, each having an alpha channel, into a destination bitmap. The destination bitmap may be the frame buffer...(col. 2, lines 31-33). {The 'alpha channel' contains the alpha value, which by definition represents the transparency or opacity of the image pixel. Also, the 'frame buffer or the bit map' is interpreted to include the "*image buffer*" where the "*first stream of image pixels*" is stored.}

(c) "*a mixing unit configured to read a first stream of image pixels from the image buffer, read a second stream of pixels form the accumulation buffer, blend each image pixel with the corresponding accumulation buffer pixel based on an alpha value provided with the image pixel*" in the following:

- For each pixel in the destination bitmap {interpreted as "*a first stream of image pixel from the image buffer*"}, the present invention processes the layers having a corresponding pixel...accumulating color and alpha values {interpreted as "*blend each image pixel with the corresponding accumulation buffer pixel based on an alpha value provided with the image pixel*"} (col. 2, lines 34-37).
- As each pixel's data is read, it is merged with the current value of accumulator using a compositing method...accumulates alpha values as well as color values (col. 5, lines 1-5). {Interpreted broadly to read as "*to read a first stream of image pixels from the image buffer, read a second*

stream of pixels form the accumulation buffer, blend each image pixel with the corresponding accumulation buffer pixel based on an alpha value provided with the image pixel"}.

- Processor identifies a pixel in layer having a position corresponding to the image pixel being rendered, and merges the color value of the identified pixel with the current value of accumulator...processor also merges the alpha value of the identified pixel with an alpha value stored in accumulator (col. 5, lines 41-46) {'Processor' is the "*mixing unit*" that blends the first stream of image pixels with the existing stream of image pixel in the accumulation buffer based on the corresponding alpha value}.
- For at least one image pixel (col. 10, line 52). {Interpreted as "*a first stream of image pixels from the image buffer*"}.
- Compositing the color value of the layer pixel with the accumulator color value (col. 10, lines 57-58). {Interpreted as "*read a second stream of pixels from the accumulation buffer, blend each image pixel with the corresponding accumulation buffer pixel*"}.
- Further comprises compositing the opacity value of the layer pixel with the accumulator opacity value (col. 11, lines 8-9). {Interpreted as "*blend each image pixel with the corresponding accumulation buffer pixel based on an alpha value provided with the image pixel*"}.

(d) "*generate a third stream of output pixels wherein the third stream of output pixels are transferred to the accumulation buffer*" in the following:

- Storing the result in the accumulator (col. 10, line 59). {Interpreted as "*generate a third stream of output pixels wherein the third stream of output pixels are transferred to the accumulation buffer*"}.
- A compositor coupled to the layer selector and to the accumulator...compositing the color value of the layer pixel with the accumulator color value and storing the result in the accumulator (col. 11, lines 23-27). {'A compositor' is the "*mixing unit*" that performs the following: "*read a first stream of image pixels from the image buffer, read a second stream of pixels form the accumulation buffer, blend each image pixel with the corresponding accumulation buffer pixel based on an alpha value provided with the image pixel, and thus, generate a third stream of output pixels wherein the third stream of output pixels are transferred to the accumulation buffer*"}.

In reference to claim 5, Brunner et al. discloses all limitations of claim 1 as described in the current paragraph above. In addition, Brunner et al. discloses the limitation of "*the image buffer resides within the frame buffer of a graphics system*" in the following:

- The present invention renders two or more overlapping layers, each having an alpha channel, into a destination bitmap. The destination bitmap may be the frame buffer...(col. 2, lines 31-33). {The 'frame buffer or the bit

map' is interpreted as to include the "*image buffer*" where the "*first stream of image pixels*" is stored.}

In reference to claim 7, the applicant claims "*a method*" comprising *(a), (b), (c), and (d)* limitations. These limitations of the current claim are interpreted to be the same limitations cited in claim 1, and thus the only difference between claim 1 and 7 is that claim 1 cites "*a system*" while claim 7 cites "*a method*". Therefore, claim 7 is rejected using the same references and interpretations used to reject claim 1 above.

In reference to claim 9, Brunner et al. discloses all limitations of claim 7 as described above. In addition, Brunner et al. discloses the limitation of "*said blending comprises blending red, green and blue components of each output pixel in parallel* " in the following:

- Each layer contains a plurality of pixels, each pixel having a color value...according to a conventional color-encoding scheme, RGB...several pixels may be processed in parallel using a number of accumulators (col. 4, lines 1-2, 26-49). {Since each pixels include a color value of red, green or blue, processing several pixels in parallel will comprise "*blending red, green, and blue components of each output pixel in parallel*"}.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunner et al., U.S. Patent No. 6,369,830 in view of the on-line publication entitled, "Advanced Graphics Programming Techniques Using Open GL" by McReynolds et al.

In reference to claim 2, Brunner et al. discloses all limitations of claim 1 as described in paragraph 3 above but does not explicitly disclose the limitations of "*the color precision of the accumulation buffer is greater than the color precision of the image buffer*". McReynolds et al. discloses the said limitation in the following:

- McReynolds et al. discloses in the definition of 'blending with the accumulation buffer' that 'in order to maintain accuracy over many blending operations, the accumulation buffer has a higher number of bits per color components than a typical color buffer' (section 6.4, lines 3-4). {Higher number of bits per color components will result in greater color precision for the accumulation buffer}.

It would have been obvious to someone of ordinary skill in the art to take the teachings of Brunner et al. and add the limitation of "*the color precision of the accumulation buffer is greater than the color precision of the image buffer*" from McReynolds et al. in order to maintain color precision accuracy over many blending operations.

In reference to claim 6, Brunner as described in paragraph 3 above discloses all limitations of claim 1 but does not explicitly disclose the limitation of "*the color precision of the accumulation buffer is at least ΔN larger than the color precision of the image buffer, wherein ΔN is the base two logarithm of the maximum number of images to be blended into the accumulation buffer*". McReynolds et al. discloses the said limitation in the following:

- McReynolds et al. discloses in the definition of 'blending with the accumulation buffer' that 'in order to maintain accuracy over many blending operations, the accumulation buffer has a higher number of bits per color components than a typical color buffer (section 6.4, lines 3-4). {'Higher number of bits per color components than a typical color buffer' is interpreting broadly as to include the bit range "*ΔN larger than the color precision of the image buffer*". The definition of *ΔN*, base two log of maximum number of images to be blended into the accumulation buffer, is one of design choices resulting in the accumulation buffer having a higher number of bits per color than the image buffer. DN as defined by the applicant has no clear advantage over other design choices, and the

specific definition still falls under the range of bit size disclosed by McReynolds}.

It would have been obvious to someone of the ordinary skill in the art to take the teachings of Brunner et al. and to take from McReynolds et al. and one of many design choices to modify the bit size of the accumulation buffer to be at least ΔN larger than that of the image buffer, where ΔN is defined as stated in the claim language, in order to maintain color precision accuracy over many blending operations.

In reference to claim 8, the same basis for rejection as applied to claim 2 is used to reject the current claim.

7. Claims 3, 4, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunner et al. in view of Tang et al., U.S. Patent Publication No. 2003/0160789.

In reference to claim 3, Brunner et al. discloses all limitations of claim 1 as described in the current paragraph above but does not explicitly disclose all limitations of "*the mixing unit includes a plurality of mixing circuits, wherein each mixing circuit operates on a corresponding color components*". Brunner et al. in view of Tang et al. discloses the said limitation in the following:

- Brunner et al. discloses the following: 'Each layer contains a plurality of pixels, each pixel having a color value...according to a conventional color-encoding scheme, RGB...each pixel also has an alpha value...several pixels may be processed in parallel using a number of accumulators' (col. 4, lines 1-2, 26-49). {'A number of accumulators' is interpreted as "*the*

mixing unit includes a plurality of mixing circuits", and since each pixel provides a RGB color component and an alpha value, each of the plurality of accumulators are capable of mixing "*a corresponding color component*"}.

- Brunner does not explicitly disclose the limitation of "*each mixing circuit operates on a corresponding color components*". Tang et al. discloses the said limitation when describing an array of memory blocks with each memory block capable of storing sample values such as red, green, blue, z, and alpha (paragraph 0131, lines 4-6). {So the individual color components are operated on separately}.

It would have been obvious to someone of ordinary skill in the art to take the teachings of Brunner et al. and to add from Tang et al. the process of mixing each of the color components separately in parallel in order to improve the speed and efficiency of the blending process. Mixing or blending each of the color components in parallel at the same time reduces blending processes to plurality of short operations, and thus it would improve the overall process time.

In reference to claim 4, Brunner et al. discloses all limitations of claim 1 as described in paragraph 3 above but does not explicitly disclose the limitation of "*the accumulation buffer resides within a texture buffer or a graphics system*". Tang et al. discloses the said limitation in the following:

- Texture buffer may be configured to store texture maps, image processing buffers, and accumulation buffers for hardware accelerator (paragraph [0106], lines 2-4).

It would have been obvious to someone of ordinary skill in the art to take the teachings of Brunner and to add from Tang et al. a texture buffer that includes the accumulation buffer eliminate the need for extra buffers and to expand the capacities of the texture buffer since a texture buffer can include several SDRAMs capable of housing several types of buffers and memories. In addition, having the accumulation buffer reside in the texture buffer will reduce interconnect lengths and thus improve speed and efficiency of the hardware accelerator.

In reference to claim 10, Brunner et al. discloses all limitations of claim 1 as described in paragraph 3 above but does not explicitly disclose the limitation of *"the method of claim 7, wherein (a), (b), (c) and (d) are performed by a graphics hardware accelerator chip in response to software functions executed on a host processor"*. Brunner et al. in view of Tang et al. discloses the said limitation in the following:

- Although Brunner et al. does not explicitly disclose a *"hardware accelerator"*, the prior art discloses the overall architecture of one embodiment where the system is implemented on a conventional personal computer having a central processing unit and/or graphics processor...(col. 3, lines 36-39). {A system having a CPU and/or graphics processor can be interpreted to include a *"host processor"* that instructs the *"graphics hardware accelerator"* to perform *(a), (b), (c) and (d)*. Also,

the instruction is given via software since that is the conventional method of communication between the CPU and the graphics processor}.

- In addition, Tang et al. discloses a hardware accelerator that may receive geometric parameters defining primitives such as triangles from media processor, and render the primitives in terms of samples (paragraph [0115], lines 1-4). {In this case, the hardware accelerator receives input image pixels and blends the image pixels in terms of a pixel color component}.

It would have been obvious to someone of ordinary skill in the art to take the teachings of Brunner et al. and to add from Tang et al. a graphics hardware accelerator in order to have a separate processor that performs the blending function using the accumulation buffer. With this improvement, the CPU is not taxed by the blending function and gains improvements in speed and efficiency.

In reference to claim 11, the same basis for rejection as applied to claims 1, 4, and 7 is used to reject the current claim.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brunner et al. in view of Tang et al. as applied to claim 11 above, and further in view of Marino, U.S. Patent Publication No. 2003/0137523. Bruner et al. in view of Tang et al. discloses all limitations of claim 11 as describe in paragraph 11 above but does not explicitly disclose the limitations of "*wherein the texture buffer has a configurable pixel depth precision*". Bruner et al. in view of Marino discloses the said limitation of in the following:

- From Brunner et al.: Texture buffer may include several SDRAMs...Texture buffer may have many different capacities (paragraph [0106], lines 1-5). {"*Pixel depth precision*" refers to the number colors represented by the pixel or the number of bits per color. Since Brunner et al. discloses a texture buffer with several SDRAMs and many different capacities, Brunner et al. discloses the said limitation}.
- From Marino: The invention includes a graphics system blending unit that bit slices multipliers, e.g., such as an 8x8 multiplier, so at least two multiplier operations can be performed per cycle per multiplier...plurality of multipliers, and the means for reconfiguring each multiplier of the blending unit to perform at least two operations per cycle (paragraph [0011]-[0015]). {Marino discloses a method to reconfigure 'multipliers' to corresponding bit size of the image pixels to be blended together. In this embodiment, Marino discloses "*a configurable pixel depth precision*"}.

It would have been obvious to someone of ordinary skill in the art to take the teachings of Brunner et al. in view of Tang et al. and to add from Marino configurable pixel depth precision in order to gain more efficient performance using less memory allocation. Using configurable pixel depth precision eliminates waste by using appropriate size multipliers and memory space to blend image pixels.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following prior arts disclose the limitation of image blending and frame buffer.

U.S. Patent No.	Inventor(s)
6,330,002	Yamada, Toru
5,754,186	Tam, T. et. al.
6,469,710	Shum, HY et al.

The following prior arts disclose the limitations of image blending and accumulation buffer.

U.S. Patent No.	Inventor(s)
6,633,297	McCormack, J.J. et al.
6,608,630	MacInnis, A.G. et al.
U.S. Patent Publication No.	Inventor(s)
2002/0030694	Ebihara, H. et al.

Non-Patent Document

Haeberli, P. and Akeley, AK. "The Accumulation Buffer: Hardware Support for High-Quality Rendering. In Computer Graphics" (SIGGRAPH 90 Conference Proceedings), pages 309--318, 1990. 1, 2.2, 4.1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hwa C Lee whose telephone number is 703-305-8987. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on 703-3900. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9700.

Hwa C Lee
Examiner
Art Unit 2672

HCL